

WHAT IS CLAIMED IS:

1. An input stage of an analog to digital converter comprising :
an array of differential amplifiers whose differential inputs are connected to interpolated voltage taps and to an signal input,
wherein each differential amplifier has a first differential input connected to the same interpolated voltage tap as a neighboring amplifier, and a second differential input shifted by an integer number of interpolated voltage taps from the neighboring amplifier, and
wherein a zero crossing of outputs of the differential amplifiers represents the signal input.
2. The input stage of claim 1, wherein a total number of interpolated voltage taps is approximately 2^{N-1} for an N-bit analog to digital converter.
3. The input stage of claim 1, wherein a total number of interpolated voltage taps ladder is approximately 2^{N-2} for an N-bit analog to digital converter.
4. The input stage of claim 1, wherein a total number of interpolated voltage taps is approximately 2^{N-3} for an N-bit analog to digital converter.
5. The input stage of claim 1, wherein the interpolated voltage taps are based on taps from a reference ladder.
6. The input stage of claim 1, wherein each differential input of each differential amplifier is connected to a capacitor.

7. The input stage of claim 6, wherein each capacitor includes at least two sub-capacitors.

8. The input stage of claim 1, wherein at least one of the differential amplifiers has a positive differential input connected to a negative differential input of one neighboring differential amplifier, and a negative differential input connected to a positive differential input of another neighboring differential amplifier.

9. The input stage of claim 1, wherein each differential input of each differential amplifier shares an input capacitor with an opposite polarity input of a neighboring amplifier.

10. The input stage of claim 1, wherein the analog to digital converter is a flash converter.

11. The input stage of claim 1, wherein the analog to digital converter is a subranging converter.

12. The input stage of claim 1, wherein the analog to digital converter is a folding converter.

13. The input stage of claim 1, further including a plurality of comparators configured to latch the outputs of the differential amplifiers array as inputs, and configured to output signals to an encoder to be converted to N-bit output.

14. An input stage of an analog to digital converter comprising :
a plurality of differential amplifiers whose differential inputs are connected to interpolated voltage taps and to an signal input,

wherein any pair of neighboring differential amplifiers has one set of differential inputs of the same polarity connected to the same interpolated voltage tap, and one set of differential inputs of the same polarity connected to a different interpolated voltage taps, and

wherein a zero crossing of outputs of the differential amplifiers represents the signal input.

15. The input stage of claim 14, wherein a total number of interpolated voltage taps is approximately 2^{N-1} for an N-bit analog to digital converter.

16. The input stage of claim 14, wherein a total number of interpolated voltage taps is approximately 2^{N-2} for an N-bit analog to digital converter.

17. The input stage of claim 14, wherein a total number of interpolated voltage taps is approximately 2^{N-3} for an N-bit analog to digital converter.

18. The input stage of claim 14, wherein the interpolated voltage taps are based on taps from a reference ladder.

19. The input stage of claim 14, wherein each differential input to each amplifier is connected to a capacitor.

20. The input stage of claim 19, wherein each capacitor includes at least two sub-capacitors.

21. The input stage of claim 14, wherein at least one of the amplifiers has a positive differential input connected to a negative differential input of one neighboring differential amplifier, and a negative differential input

connected to a positive differential input of another neighboring differential amplifier.

22. The input stage of claim 14, wherein each differential input of each amplifier shares an input capacitor with an opposite polarity input of a neighboring amplifier.

23. The input stage of claim 14, wherein the analog to digital converter is a flash converter.

24. The input stage of claim 14, wherein the analog to digital converter is a subranging converter.

25. The input stage of claim 14, wherein the analog to digital converter is a folding converter.

26. The input stage of claim 14, further including a plurality of comparators configured to latch the outputs of the differential amplifiers array as inputs, and configured to output signals to an encoder to be converted to N-bit output.

27. An input stage of an analog to digital converter comprising:
an array of differential amplifiers whose inputs are connected to interpolated voltage taps and to an signal input,

wherein each amplifier has a first polarity input corresponding to one interpolated tap such that adjacent amplifiers share the one interpolated voltage tap, and

wherein each amplifier has a second polarity input such that adjacent amplifiers are connected to other interpolated voltage taps, and

wherein a zero crossing of outputs of the differential amplifiers represents the signal input.

28. The input stage of claim 27, wherein a total number of interpolated voltage taps is approximately 2^{N-1} for an N-bit analog to digital converter.

29. The input stage of claim 27, wherein a total number of interpolated voltage taps is approximately 2^{N-2} for an N-bit analog to digital converter.

30. The input stage of claim 27, wherein a total number of interpolated voltage taps is approximately 2^{N-3} for an N-bit analog to digital converter.

31. The input stage of claim 27, wherein the interpolated voltage taps are based on taps from a reference ladder.

32. The input stage of claim 27, wherein each input to each amplifier is connected to a capacitor.

33. The input stage of claim 32, wherein each capacitor includes at least two sub-capacitors.

34. The input stage of claim 27, wherein at least one of the amplifiers has the first polarity input connected to the second polarity input of one neighboring amplifier, and the second polarity input connected to a the first polarity input of another neighboring amplifier.

35. The input stage of claim 27, wherein each input of each differential amplifier shares an input capacitor with an opposite polarity input of a neighboring amplifier.

36. The input stage of claim 27, wherein the analog to digital converter is a flash converter.

37. The input stage of claim 27, wherein the analog to digital converter is a subranging converter.

38. The input stage of claim 27, wherein the analog to digital converter is a folding converter.

39. The input stage of claim 27, further including a plurality of comparators that input the outputs of the amplifiers, and output them to an encoder to be converted to N-bit output.

40. An input stage of an analog to digital converter comprising:
a plurality of amplifiers whose inputs are connected to a plurality of interpolated voltage taps and to an signal input,
wherein each amplifier has inputs shifted by a fraction of an interpolated voltage tap relative to its adjacent amplifier, and
wherein a zero crossing of outputs of the differential amplifiers represents the signal input.